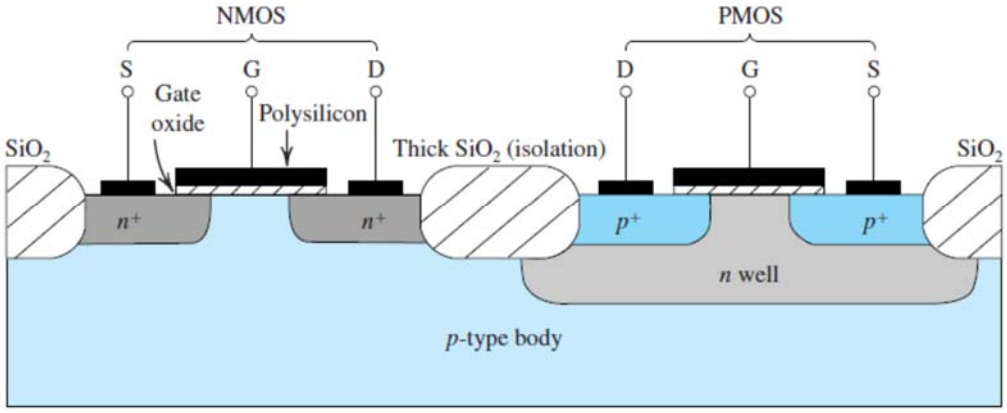
Complementary MOS or CMOS:

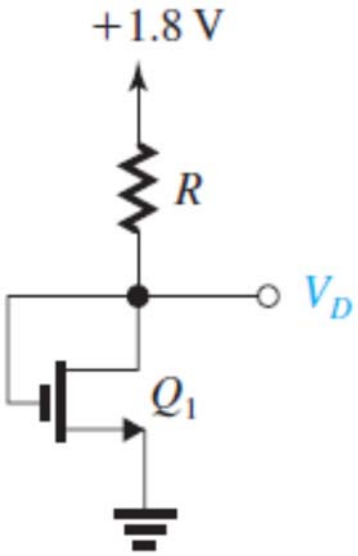


- As the name implies, complementary MOS technology employs MOS transistors of both polarities.
- Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit configurations.
- Figure above shows a cross section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated.
- Observe that while the NMOS transistor is implemented directly in the p-type substrate, the PMOS transistor is fabricated in a specially created n region, known as an n well.
- The two devices are isolated from each other by a thick region of oxide that functions as an insulator.
- Not shown on the diagram are the connections made to the p-type body and to the n well. The latter connection serves as the body terminal for the PMOS transistor.

Example:

For the circuit in Fig. E5.9, find the value of R that results in $V_D = 0.7$ V. The MOSFET has $V_{tn} = 0.5$ V, $\mu_n C_{ox} = 0.4$ mA/V^2, $W/L = \dfrac{0.72\ \mu\text{m}}{0.18\ \mu\text{m}}$, and $\lambda = 0$.

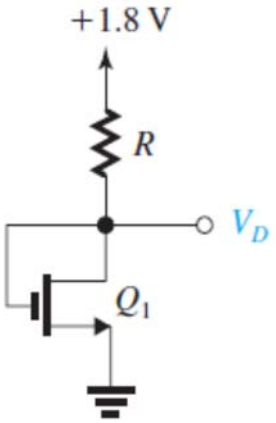
Solution:

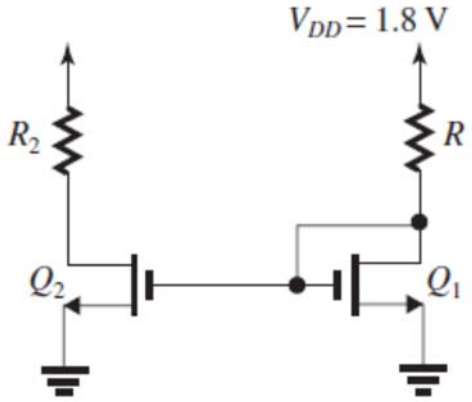


Example:

Figure E5.10 shows a circuit obtained by augmenting the circuit of Fig. E5.9 considered in Exercise 5.9 with a transistor Q_2 identical to Q_1 and a resistance R_2. Find the value of R_2 that results in Q_2 operating at the edge of the saturation region. Use your solution to Exercise 5.9.

Solution:

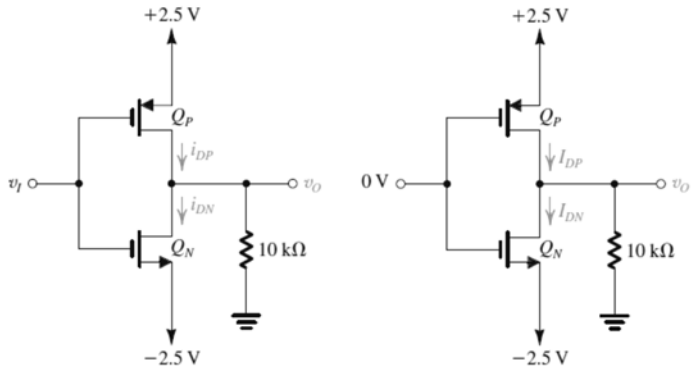


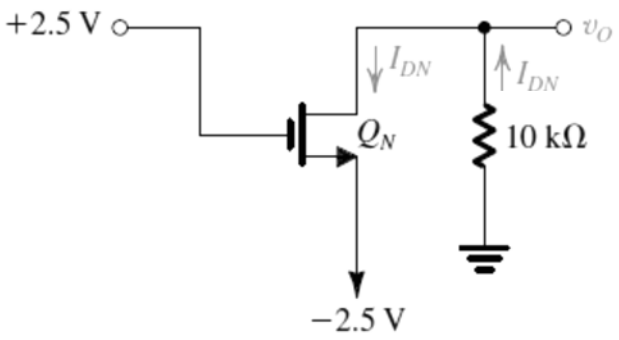


Example:

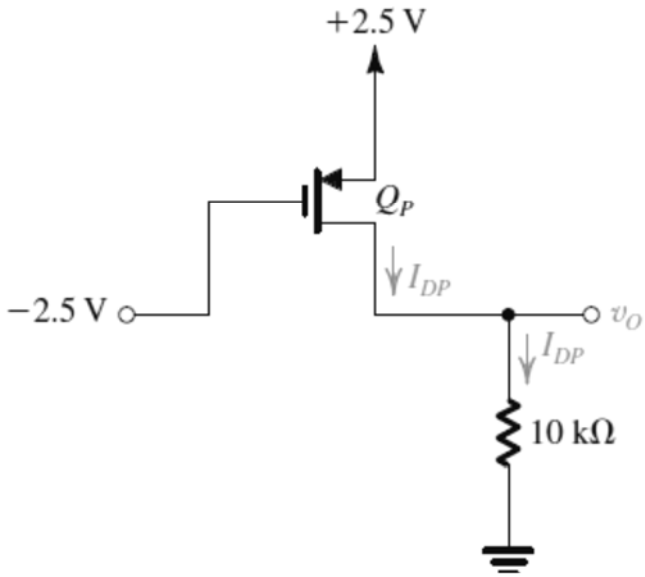
The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1$ mA/V^2 and $V_{tn} = -V_{tp} = 1$ V. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0$ V, +2.5 V, and −2.5 V.

Solution:





(c)

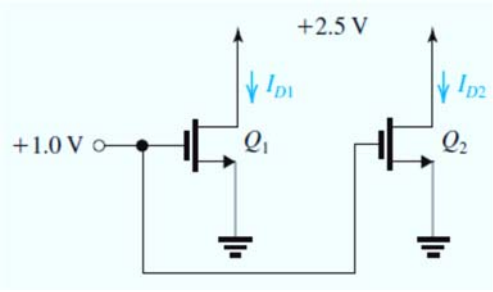


Example:

5.29 Figure P5.29 shows two NMOS transistors operating in saturation at equal V_{GS} and V_{DS}.

(a) If the two devices are matched except for a maximum possible mismatch in their W/L ratios of 3%, what is the maximum resulting mismatch in the drain currents?

(b) If the two devices are matched except for a maximum possible mismatch in their V_t values of 10 mV, what is the maximum resulting mismatch in the drain currents? Assume that the nominal value of V_t is 0.6 V.



Solution:

Example:

D 5.32 In a particular IC design in which the standard channel length is 1 μm, an NMOS device with W/L of 10 operating at 200 μA is found to have an output resistance of 100 kΩ, about $\frac{1}{5}$ of that needed. What dimensional change can be made to solve the problem? What is the new device length? The new device width? The new W/L ratio? What is V_A for the standard device in this IC? The new device?

Example:

D 5.33 For a particular n-channel MOS technology, in which the minimum channel length is 0.5 μm, the associated value of λ is 0.03 V^{-1}. If a particular device for which L is 1.5 μm operates in saturation at $v_{DS} = 1$ V with a drain current of 100 μA, what does the drain current become if v_{DS} is raised to 5 V? What percentage change does this represent? What can be done to reduce the percentage by a factor of 2?