ENSC 225 (2016-2) Laboratory #3
Characterization of BJTs and single stage BJT amplifier
Due: July 13, 11:59pm

Read this lab handout thoroughly before you start the experiment.

You will be using the CA3046 npn-BJT array and the 2907 discrete pnp transistor. The 3046 array is an integrated chip consisting of 5 npn-BJTs in a 14 pin DIP package. The BJTs are produced by the Classical Bipolar Technology which uses the reverse bias of a p-n junction to isolate the individual transistors in the chip. Therefore, the silicon substrate of chip has to be maintained at the lowest potential in the circuit. In 3046 chip the substrate is pin 13. This pin also serves as the emitter contact of the BJT Q5 in that package. So, for the characterization experiments given below you should not use the transistor Q5. You should choose any one among Q1 through Q4. The pin 13 has to be connected to the most negative potential in the circuit.

Please operate the SPA with extreme care

1. NPN transistor Characteristics

Use the SPA to plot the I_C vs V_{CE} characteristics of an npn transistor. The SPA has been pre-wired to use the transistor Q1 as the Device-Under-Test. SMU1, 2 and 3 are physically connected to pins 3, 2 and 1, respectively, of the chip holder. This connection represents the collector, base and emitter of Q1. The pin#27 of the chip carrier (ZIF socket) will have the pin13 of the chip and this pin is connected to SMU4. Please verify this connection before you start the experiment.

Place the CA3046 chip in the ZIF socket and clamp the pins.
Turn on the SPA and select BJT characterization mode
This will set the SMU1 as Emitter, SMU2 as Base and SMU3 as collector
Navigate to SMU4 and set the following:

VNAME as VS
INAME as IS
MODE as V
FCTN as CONST

With this setting now go the sweep setting screen
You will observe the following:

VAR-1 set for VCE
VAR-2 set for IB
SMU4 not set

Set the VAR-1 to sweep 0 to 5V in 25mV steps. This should give you a total of 201 steps
Set VAR-2, the I_B, Start value 0μA, step value 2μA and a total number of steps of 15
Set SMU4 Source value as 0V
This should give you 15 sweeps of 201 data points for each sweep.

You need not set the plotting scale, you can go straight to the graph and press the “SINGLE” to let the SPA sweep and plot the BJT characteristics. The plot may not be properly scaled. Once the sweeping is done, using the following on-screen menu selection you can auto-scale it in two simple button pushes.

After the single sweep process is complete, press the "SCALING" from the bottom of the screen menu selection. Then you press the "AUTO SCALING" button from the right side of the screen menu selection buttons. This will automatically scale the plot and give you the formatted I_C vs V_{CE} characteristics on the screen.

Transfer the data to the computer and eventually to your USB memory stick. Since this is a large text file, the data transfer takes a while. Be patient.

2. PNP transistor Characteristics

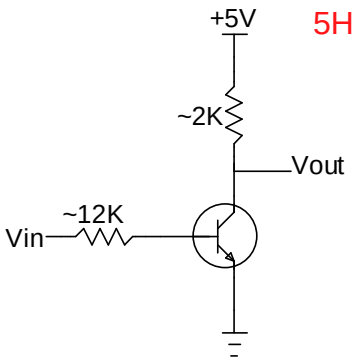
Remove the 3046 chip and place the pnp transistor 2907, such that pins 1, 2 and 3 of the socket is connecting the collector, base and emitter respectively. Set the SPA to scan V_{CE} from 0 to -3V and I_B from 0 in -10μA steps for 15 sweeps. Graph the characteristics and transfer the data for your records.

3. Forward current gain (β) and Early Voltage determination

a) Using the data from SPA, plot the I_C vs V_{CE} characteristics of the npn and pnp transistors
b) Determine, from the graph, the DC β and the early voltage for npn transistor at I_C=500μA, 1mA and 2mA @ V_{CE}=3V
c) Determine, from the graph, the DC β and the early voltage for pnp transistor at I_C= 5mA and 10mA @ V_{EC}=2V.
d) Compare these with the datasheet published values

4. Large signal characteristics

Using the circuit shown below plot the large signal characteristics of the npn transistor. Apply a slow varying input signal, for example a 0 to 5V triangular waveform at 5Hz ~~10 Hz~~ or alternatively you may use the second voltage source in the power supply to apply the input voltage in steps and collect the input and corresponding output voltages. If you are using the function generator to apply the input voltage, ensure the signal is from 0 to 5V when the function generator is connected to the circuit. Make sure you collect sufficient number of data for the input voltage from 0 to 5V. [Remember to connect the pin 13 of the chip to Gnd during this experiment]



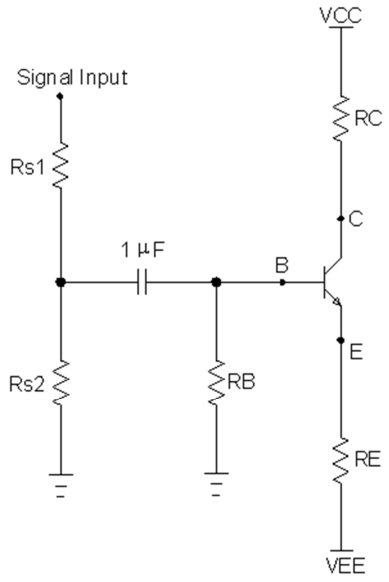
Plot the large signal transfer characteristics: Output versus the input voltage. Also, draw the load line for this circuit on the npn I_C vs V_{CE} characteristics. Graphically, determine the large signal characteristics from the load line graph and compare that with the experimental data. Explain any discrepancies that you observe.

5. Single stage transistor amplifier

Design a single stage common emitter amplifier with a DC collector current of 500μA and a DC collector voltage of 3V. Choose the appropriate resistors to bias the transistor using for a ± 9V DC power supply. [Remember to connect the pin 13 of the chip to -9V (V_{EE})]

Choose R_{S1} and R_{S2} such that you can input and few-millivolt signal to the base. Wire the circuit neatly and compactly on the bread board. Do not string several resistors to make-up a value. If your calculated value is not available in the bin choose the nearest available value and recalculate your bias.

For Section-4: If you use the FnGen to obtain the large signal transfer characteristics, make sure you trigger the scope output properly, average the signal and get the scope screen data in excel format.



Measurements and calculations:

a. Using DMM, measure the (DC) supply voltages and voltages at nodes B, C and E
b. Based on the Bias voltage measurements, determine the transistor currents
c. Determine the DC β of the transistor. Compare this β value from the SPA plot
d. Apply a small signal input and observe the output at 1 kHz. If necessary, you can use a voltage divider to reduce the function generator output voltage.
e. Compute the gain (small signal $\mathcal{V}_C/\mathcal{V}_B$)
f. By-pass the emitter resistor using the largest available electrolytic capacitor in your parts bag
g. Measure the input and output peak-to-peak voltages and compute the gain again
h. Determine the maximum output peak-to-peak voltage swing you can get without distortion
i. For the emitter by-passed circuit configuration, perform a frequency response test. Set the output peak-to-peak voltage swing around 2V at 1 kHz. Sweep the frequency from 10Hz to 2MHz and collect the input and output values at frequent intervals. Plot a frequency response (Bode Plot) of your amplifier (Phase plot is not necessary)
j. Simulate your amplifier circuit using LT-Spice. You have to input the CA3046 spice parameters and create the BJT in LT-Spice. Obtain the DC operating points and compare this with your experimental bias values
k. Using LT-Spice run a frequency response simulation and plot the frequency response. Compare the experimental frequency response and the simulated response
l. Construct the small signal model for this circuit and compare the model-predicted mid-band gain, simulated mid-band gain and the experimental mid-band gain values.
m. Bring the input signal to 1 kHz. Make sure the output is 2V pk-to-pk.
n. Now increase the input amplitude slowly. Determine which portion of the output signal first shows signal distortion? Do the same for your LT-Spice model and compare the performance of your actual circuit to the simulation. Describe this behavior based on your bias values.

Capture necessary scope waveforms to include in your write-up. A good portion of the marks will be assigned to the design of the amplifier that gives the specified collector current and the maximum undistorted output voltage swing. You have to demo the working circuit to a TA or the instructor.

Write a formal report addressing the five sections of this lab exercise.