voltage of approximately 0.2 V.

(a) Specify V_{DS} at the bias point.
(b) What is the gain achieved? What is the signal amplitude $\hat{v}_{gs}$ that results in the 0.5-V signal amplitude at the output?
(c) If the dc bias current in the drain is to be 100 μA, what value of R_D is needed?
(d) If $k_n' = 200\ \mu\text{A/V}^2$, what W/L ratio is required for the MOSFET?

***7.9** Figure P7.9 shows an amplifier in which the load resistor R_D has been replaced with another NMOS transistor Q_2 connected as a two-terminal device. Note that because v_{DG} of Q_2 is zero, it will be operating in saturation at all times, even when $v_I = 0$ and $i_{D2} = i_{D1} = 0$. Note also that the two transistors conduct equal drain currents. Using $i_{D1} = i_{D2}$, show that for the range of v_I over which Q_1 is operating in saturation, that is, for

$$V_{t1} \le v_I \le v_O + V_{t1}$$

the output voltage will be given by

$$v_O = V_{DD} - V_t + \sqrt{\frac{(W/L)_1}{(W/L)_2}}V_t - \sqrt{\frac{(W/L)_1}{(W/L)_2}}v_I$$

where we have assumed $V_{t1} = V_{t2} = V_t$. Thus the circuit functions as a linear amplifier, even for large input signals. For $(W/L)_1 = (50\ \mu\text{m}/0.5\ \mu\text{m})$ and $(W/L)_2 = (5\ \mu\text{m}/0.5\ \mu\text{m})$, find the voltage gain.

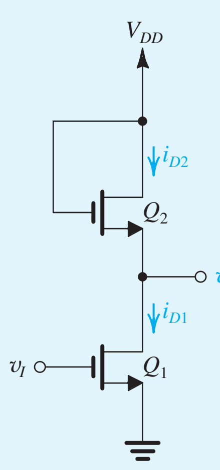

Figure P7.9

7.10 A BJT amplifier circuit such as that in Fig. 7.6 is operated with $V_{CC} = +5$ V and is biased at $V_{CE} = +1$ V. Find the voltage gain, the maximum allowed output negative swing without the transistor entering saturation, and the corresponding maximum input signal permitted.

7.11 For the amplifier circuit in Fig. 7.6 with $V_{CC} = +5$ V and $R_C = 1\ \text{k}\Omega$, find V_{CE} and the voltage gain at the following dc collector bias currents: 0.5 mA, 1 mA, 2.5 mA, 4 mA, and 4.5 mA. For each, give the maximum possible positive- and negative-output signal swing as determined by the need to keep the transistor in the active region. Present your results in a table.

D 7.12 Consider the CE amplifier circuit of Fig. 7.6 when operated with a dc supply $V_{CC} = +5$ V. It is required to find the point at which the transistor should be biased; that is, find the value of V_{CE} so that the output sine-wave signal v_{ce} resulting from an input sine-wave signal v_{be} of 5-mV peak amplitude has the maximum possible magnitude. What is the peak amplitude of the output sine wave and the value of the gain obtained? Assume linear operation around the bias point. (*Hint:* To obtain the maximum possible output amplitude for a given input, you need to bias the transistor as close to the edge of saturation as possible without entering saturation at any time, that is, without v_{CE} decreasing below 0.3 V.)

7.13 A designer considers a number of low-voltage BJT amplifier designs utilizing power supplies with voltage V_{CC} of 1.0, 1.5, 2.0, or 3.0 V. For transistors that saturate at $V_{CE} = 0.3$ V, what is the largest possible voltage gain achievable with each of these supply voltages? If in each case biasing is adjusted so that $V_{CE} = V_{CC}/2$, what gains are achieved? If a negative-going output signal swing of 0.4 V is required, at what V_{CE} should the transistor be biased to obtain maximum gain? What is the gain achieved with each of the supply voltages? (Notice that all of these gains are independent of the value of I_C chosen!)

D *7.14 A BJT amplifier such as that in Fig. 7.6 is to be designed to support relatively undistorted sine-wave output signals of peak amplitudes P volt without the BJT entering saturation or cutoff and to have the largest possible voltage gain, denoted A_v V/V. Show that the minimum supply voltage V_{CC} needed is given by

$$V_{CC} = V_{CEsat} + P + |A_v|V_T$$

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

Also, find V_{CC}, specified to the nearest 0.5 V, for the following situations:

(a) $A_v = -20$ V/V, $P = 0.2$ V
(b) $A_v = -50$ V/V, $P = 0.5$ V
(c) $A_v = -100$ V/V, $P = 0.5$ V
(d) $A_v = -100$ V/V, $P = 1.0$ V
(e) $A_v = -200$ V/V, $P = 1.0$ V
(f) $A_v = -500$ V/V, $P = 1.0$ V
(g) $A_v = -500$ V/V, $P = 2.0$ V

7.15 The transistor in the circuit of Fig. P7.15 is biased at a dc collector current of 0.3 mA. What is the voltage gain? (*Hint:* Use Thévenin's theorem to convert the circuit to the form in Fig. 7.6.)

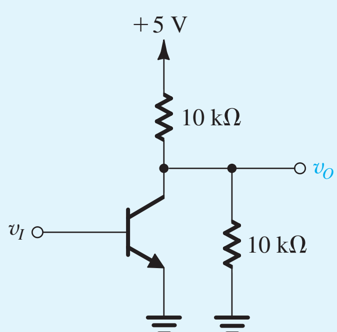

Figure P7.15

7.16 Sketch and label the voltage-transfer characteristics of the *pnp* amplifiers shown in Fig. P7.16.

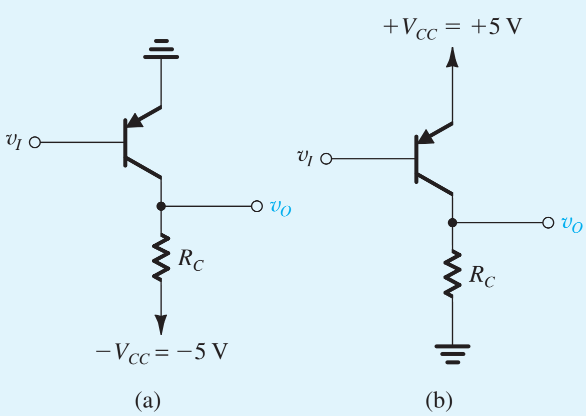

Figure P7.16

***7.17** In deriving the expression for small-signal voltage gain A_v in Eq. (7.21) we neglected the Early effect. Derive this expression including the Early effect by substituting

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

in Eq. (7.4) and including the factor $\left(1 + V_{CE}/V_A\right)$ in Eq. (7.11). Show that the gain expression changes to

$$A_v = \frac{-I_C R_C/V_T}{\left[1 + \dfrac{I_C R_C}{V_A + V_{CE}}\right]} = -\frac{\left(V_{CC} - V_{CE}\right)/V_T}{\left[1 + \dfrac{V_{CC} - V_{CE}}{V_A + V_{CE}}\right]}$$

For the case $V_{CC} = 5$ V and $V_{CE} = 3$ V, what is the gain without and with the Early effect taken into account? Let $V_A = 100$ V.

7.18 When the amplifier circuit of Fig. 7.6 is biased with a certain V_{BE}, the dc voltage at the collector is found to be +2 V. For $V_{CC} = +5$ V and $R_C = 1$ kΩ, find I_C and the small-signal voltage gain. For a change $\Delta v_{BE} = +5$ mV, calculate the resulting Δv_O. Calculate it two ways: by using the transistor exponential characteristic Δi_C, and approximately, using the small-signal voltage gain. Repeat for $\Delta v_{BE} = -5$ mV. Summarize your results in a table.

***7.19** Consider the amplifier circuit of Fig. 7.6 when operated with a supply voltage $V_{CC} = +3$V.

(a) What is the theoretical maximum voltage gain that this amplifier can provide?
(b) What value of V_{CE} must this amplifier be biased at to provide a voltage gain of –60 V/V?
(c) If the dc collector current I_C at the bias point in (b) is to be 0.5 mA, what value of R_C should be used?
(d) What is the value of V_{BE} required to provide the bias point mentioned above? Assume that the BJT has $I_S = 10^{-15}$ A.
(e) If a sine-wave signal v_{be} having a 5-mV peak amplitude is superimposed on V_{BE}, find the corresponding output voltage signal v_{ce} that will be superimposed on V_{CE} assuming linear operation around the bias point.
(f) Characterize the signal current i_c that will be superimposed on the dc bias current I_C.

(g) What is the value of the dc base current I_B at the bias point? Assume $\beta = 100$. Characterize the signal current i_b that will be superimposed on the base current I_B.

(h) Dividing the amplitude of v_{be} by the amplitude of i_b, evaluate the incremental (or small-signal) input resistance of the amplifier.

(i) Sketch and clearly label correlated graphs for v_{BE}, v_{CE}, i_C, and i_B versus time. Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

7.20 The essence of transistor operation is that a change in v_{BE}, Δv_{BE}, produces a change in i_C, Δi_C. By keeping Δv_{BE} small, Δi_C is approximately linearly related to Δv_{BE}, $\Delta i_C = g_m \Delta v_{BE}$, where g_m is known as the transistor transconductance. By passing Δi_C through R_C, an output voltage signal Δv_O is obtained. Use the expression for the small-signal voltage gain in Eq. (7.20) to derive an expression for g_m. Find the value of g_m for a transistor biased at $I_C = 0.5$ mA.

7.21 The purpose of this problem is to illustrate the application of graphical analysis to the circuit shown in Fig. P7.21. Sketch $i_C - v_{CE}$ characteristic curves for the BJT for $i_B = 10$ μA, 20 μA, 30 μA, and 40 μA. Assume the lines to be horizontal (i.e., neglect the Early effect), and let $\beta = 100$. For $V_{CC} = 5$ V and $R_C = 1$ kΩ, sketch the load line. What peak-to-peak collector voltage swing will result for i_B varying over the range 10 μA to 40 μA? If the BJT is biased at $V_{CE} = \frac{1}{2} V_{CC}$, find the value of I_C and I_B. If at this current $V_{BE} = 0.7$ V and if $R_B = 100$ kΩ, find the required value of V_{BB}.

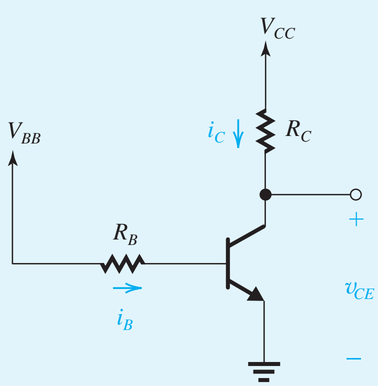

Figure P7.21

***7.22** Sketch the $i_C - v_{CE}$ characteristics of an *npn* transistor having $\beta = 100$ and $V_A = 100$ V. Sketch characteristic curves for $i_B = 20$ μA, 50 μA, 80 μA, and 100 μA. For the purpose of this sketch, assume that $i_C = \beta i_B$ at $v_{CE} = 0$. Also, sketch the load line obtained for $V_{CC} = 10$ V and $R_C = 1$ kΩ. If the dc bias current into the base is 50 μA, write the equation for the corresponding $i_C - v_{CE}$ curve. Also, write the equation for the load line, and solve the two equations to obtain V_{CE} and I_C. If the input signal causes a sinusoidal signal of 30-μA peak amplitude to be superimposed on I_B, find the corresponding signal components of i_C and v_{CE}.

Section 7.2: Small-Signal Operation and Models

***7.23** This problem investigates the nonlinear distortion introduced by a MOSFET amplifier. Let the signal v_{gs} be a sine wave with amplitude V_{gs}, and substitute $v_{gs} = V_{gs} \sin \omega t$ in Eq. (7.28). Using the trigonometric identity $\sin^2\theta = \frac{1}{2} - \frac{1}{2}\cos 2\theta$, show that the ratio of the signal at frequency 2ω to that at frequency ω, expressed as a percentage (known as the second-harmonic distortion) is

$$\text{Second-harmonic distortion} = \frac{1}{4}\frac{V_{gs}}{V_{OV}} \times 100$$

If in a particular application V_{gs} is 10 mV, find the minimum overdrive voltage at which the transistor should be operated so that the second-harmonic distortion is kept to less than 1%.

7.24 Consider an NMOS transistor having $k_n = 10\text{ mA/V}^2$. Let the transistor be biased at $V_{OV} = 0.2$ V. For operation in saturation, what dc bias current I_D results? If a 0.02-V signal is superimposed on V_{GS}, find the corresponding increment in collector current by evaluating the total collector current i_D and subtracting the dc bias current I_D. Repeat for a –0.02-V signal. Use these results to estimate g_m of the FET at this bias point. Compare with the value of g_m obtained using Eq. (7.33).

7.34 Consider a transistor biased to operate in the active mode at a dc collector current I_C. Calculate the collector signal current as a fraction of I_C (i.e., i_c/I_C) for input signals v_{be} of +1 mV, –1 mV, +2 mV, –2 mV, +5 mV, –5 mV, +8 mV, –8 mV, +10 mV, –10 mV, +12 mV, and –12 mV. In each case do the calculation two ways:

(a) using the exponential characteristic, and
(b) using the small-signal approximation.

Present your results in the form of a table that includes a column for the error introduced by the small-signal approximation. Comment on the range of validity of the small-signal approximation.

7.35 An *npn* BJT with grounded emitter is operated with $V_{BE} = 0.700$ V, at which the collector current is 0.5 mA. A 5-kΩ resistor connects the collector to a +5-V supply. What is the resulting collector voltage V_C? Now, if a signal applied to the base raises v_{BE} to 705 mV, find the resulting total collector current i_C and total collector voltage v_C using the exponential i_C–v_{BE} relationship. For this situation, what are v_{be} and v_c? Calculate the voltage gain v_c/v_{be}. Compare with the value obtained using the small-signal approximation, that is, $-g_m R_C$.

7.36 A transistor with $\beta = 100$ is biased to operate at a dc collector current of 0.5 mA. Find the values of g_m, r_π, and r_e. Repeat for a bias current of 50 μA.

7.37 A *pnp* BJT is biased to operate at $I_C = 1.0$ mA. What is the associated value of g_m? If $\beta = 100$, what is the value of the small-signal resistance seen looking into the emitter (r_e)? Into the base (r_π)? If the collector is connected to a 5-kΩ load, with a signal of 5-mV peak applied between base and emitter, what output signal voltage results?

D 7.38 A designer wishes to create a BJT amplifier with a g_m of 30 mA/V and a base input resistance of 3000 Ω or more. What collector-bias current should he choose? What is the minimum β he can tolerate for the transistor used?

7.39 A transistor operating with nominal g_m of 40 mA/V has a β that ranges from 50 to 150. Also, the bias circuit, being less than ideal, allows a ±20% variation in I_C. What are the extreme values found of the resistance looking into the base?

7.40 In the circuit of Fig. 7.20, V_{BE} is adjusted so that $V_C = 1$ V. If $V_{CC} = 3$ V, $R_C = 2$ kΩ, and a signal $v_{be} = 0.005 \sin \omega t$ volts is applied, find expressions for the total instantaneous quantities $i_C(t)$, $v_C(t)$, and $i_B(t)$. The transistor has $\beta = 100$. What is the voltage gain?

D *7.41 We wish to design the amplifier circuit of Fig. 7.20 under the constraint that V_{CC} is fixed. Let the input signal $v_{be} = \hat{V}_{be} \sin \omega t$, where $\hat{V}_{be}$ is the maximum value for acceptable linearity. For the design that results in the largest signal at the collector, without the BJT leaving the active region, show that

$$R_C I_C = (V_{CC} - 0.3) \Big/ \left(1 + \frac{\hat{V}_{be}}{V_T}\right)$$

and find an expression for the voltage gain obtained. For $V_{CC} = 3$ V and $\hat{V}_{be} = 5$ mV, find the dc voltage at the collector, the amplitude of the output voltage signal, and the voltage gain.

7.42 The table below summarizes some of the basic attributes of a number of BJTs of different types, operating as amplifiers under various conditions. Provide the missing entries. (*Note:* Isn't it remarkable how much two parameters can reveal?)

7.43 A BJT is biased to operate in the active mode at a dc collector current of 1 mA. It has a β of 100 and V_A of 100 V. Give the four small-signal models (Figs. 7.25 and 7.27) of the BJT complete with the values of their parameters.

Transistor	a	b	c	d	e	f	g
α	1.000					0.90	
β		100		∞			
I_C (mA)	1.00		1.00				
I_E (mA)		1.00				5	
I_B (mA)			0.020				1.10
g_m (mA/V)							700
r_e (Ω)				25	100		
r_π (Ω)					10.1 kΩ		

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem