Project Area Introductory Example - Backend Group

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As the backend group, our goal is to contribute improvements to the Parabix backend code generation for a particular target architecture. So far, we have mainly focused on the x86 architecture. Specifically we have focused on the extensions to x86 which include SSE2 and AVX since these extensions are the ones that introduced SIMD instructions.

One of the recent extensions are the AVX-512 extensions to AVX. Intel's announced Knights Landing processor will support these AVX-512 extensions. These extensions include instructions that make use of 512-bit registers. Some of these instructions make use of 512-bit registers to perform multiple arithmetic operations in parallel. For example, one of the instructions can perform eight 64-bit additions in parallel.

We have looked at possibly adding backend support for generating code that makes use of instructions introduced in the AVX-512 extensions. Such support could improve the backend and resulting program performance on processors that support these extensions.

One example improvement we could contribute is to add support for 512-bit addition and 512-bit transposition to Parabix. Currently, ICgrep uses SSE2 128-bit instructions when doing transposition for the x86 target architecture.

Another possible improvement would be long stream addition. ICgrep takes advantage of long integer additions. Currently LLVM implements long integer addition by using a sequence of ADDC and ADDE. It could be improved by long stream addition model. In Meng Lin’s paper [1], i256 long stream addition on AVX2 has 1.6x performance compared to LLVM addition. With AVX-512 introduced, we could improve the performance further by adopting 512-bit operations.

[1] Meng Lin's M.Sc. thesis